In the Specification:

Please replace the paragraph beginning on page 1, line 5, with the following rewritten paragraph:

~~BACKGROUND OF THE INVENTION~~

~~Field of the Invention~~

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Field of the Invention

The present invention relates to processors having compressed instructions. In particular, but not exclusively, the present invention relates to very long instruction word (VLIW) processors having compressed instructions. The present invention also relates to methods of ~~comprising~~compressing instructions for processors.

Please replace the paragraph beginning on page 3, line 26, with the following rewritten paragraph:

~~BRIEF SUMMARY OF THE INVENTION~~

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A processor embodying a first aspect of the present invention executes instructions of a program stored in compressed form in a program memory. The processor has a program counter which identifies a position in the program memory. An instruction cache has a plurality of cache blocks, each for storing one or more instructions of the program in decompressed form. A cache loading unit has a decompression section and

performs a cache loading operation in which one or more compressed-form instructions are read from the position in the program memory identified by the program counter and are decompressed and stored in one of the cache blocks of the instruction cache. A cache pointer identifies a position in the instruction cache of an instruction to be fetched for execution. An instruction fetching unit fetches an instruction to be executed from the position identified by the cache pointer. When a cache miss occurs because the instruction to be fetched is not present in the instruction cache, the instruction fetching unit causes the cache loading unit to perform its cache loading operation. An updating unit updates the program counter and cache pointer in response to the fetching of instructions so as to ensure that the position identified by the program counter is maintained consistently at the position in the program memory at which the instruction to be fetched from the instruction cache is stored in compressed form.

Please replace the paragraph beginning on page 5, line 29, with the following rewritten paragraph:

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

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Figs. 1(A), 1(B) and 1(C) show explanatory diagrams for illustrating compression of a VLIW instruction schedule;

Please replace the paragraph beginning on page 6, line 28, with the following rewritten paragraph:

~~DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS~~

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~~Fig. 1~~Fig. 2 shows parts of a processor embodying the present invention. In this example, the processor is a very long instruction word (VLIW) processor. The processor 1 includes an instruction issuing unit 10, a schedule storage unit 12, respective first, second and third execution units 14, 16 and 18, and a register file 20. The instruction issuing unit 10 has three issue slots IS1, IS2 and IS3 connected respectively to the first, second and third execution units 14, 16 and 18. A first bus 22 connects all three execution units 14, 16 and 18 to the register file 20. A second bus 24 connects the first and second units 14 and 16 (but not the third execution unit 18 in this embodiment) to a memory 26 which, in this example, is an external random access memory (RAM) device. The memory 26 could alternatively be a RAM internal to the processor 1.

Please replace the paragraph beginning on page 10, line 19, with the following rewritten paragraph:

When the processor attempts to execute the section VCS of compressed VLIW instructions the PC register 50 will initially point to the start of the section. In order to determine which instructions in the section VCS belong to the same processor packet (i.e. are instructions which must be issued simultaneously at the issue slots IS1 to IS8), and in which

positions within that packet, the compressed section VCS must be decompressed. In the instruction issuing unit 10 of Fig. 3, the section VCS is ~~compressed~~decompressed by the decompression section 44 and the resulting decompressed block of instructions DI is stored in the instruction cache 40. The clock of decompressed instructions DI corresponding to the VLIW compression section VCS is therefore not actually stored in the schedule storage unit 12 even at execution time, and at execution time the decompressed instructions DI exist only in the instruction cache 40 in an "imaginary address space".